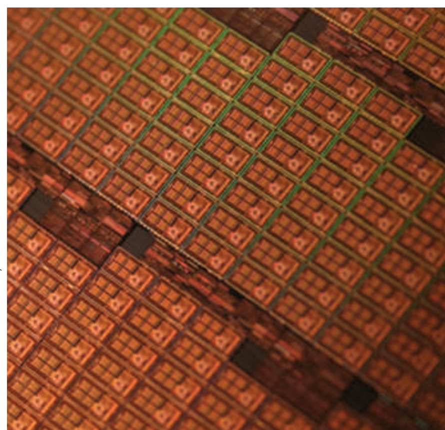
Lithography roadmap on track

Extreme UV lithography (EUVL) and 193 nm immersion lithography enhanced by double-patterning techniques will be sufficient to maintain the lithography roadmap for several technology nodes. That was the message given loud and clear at the EUVL and Immersion Extensions Symposia, which took place at the end of 2009.

The collective event, organized by the semiconductor industry consortium SEMATECH, covered technology, infrastructure and the business challenges that the industry must address for commercial manufacturing at the 22 nm half-pitch node.

Highlights from the symposia included a report from the laser developer Cymer that its laser-generated plasma sources can now generate 50 W of 13 nm EUV light at intermediate focus. High-volume commercial lithography will ultimately require around 180 W of power to expose 100 wafers per hour. Researchers also reported that 193 nm immersion lithography has successfully been extended to the 22 nm node using a variety of double-patterning approaches, including spacer, double etch and resist-freezing processes, as well as litho-etch–litho-etch and source–mask optimization schemes.



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The EUVL Symposium Steering Committee has identified three remaining areas that the industry must focus on to enable successful adoption of EUVL for commercial manufacturing. These include the availability of defect-free masks, long-term source operation with 100 W at the intermediate focus, and achievement of resist with sufficient resolution, sensitivity and line-edge roughness.

"Good progress has been made towards achieving resist resolution and sensitivity targets, with some improvement in line-edge roughness, and now chip manufacturers are demonstrating post-exposure resist processes that lead to significantly reduced line-edge roughness," said Stefan Wurm, SEMATECH's associate director of lithography.

Despite the economic climate, attendance levels surpassed those of previous years. Bryan Rice, director of lithography at SEMATECH said: "I attribute this to a combination of the industry's critical need to address the cost and risk of developing EUV technologies, and to the recognition that 22 nm solutions must be ready for insertion very soon, by 2013."

Mapper receives cash boost

Mapper Lithography, based in Delft, the Netherlands, has been awarded a subsidy of around 10 million Euros by SenterNovem, an agency of the Dutch Ministry of Economic Affairs.

Mapper will use these funds to develop a beta version of its maskless lithography tool. The tool is planned to use over 10,000 electron-beams in parallel to write patterns of electrical circuits directly onto wafers, eliminating the expensive photomask process used in current lithography machines.

The company recently shipped an electron-beam lithography platform to CEA-Leti in Grenoble, France, for use with 300-mm-diameter wafers. The machine will be used for Imagine, a three-year program that focuses on electron-beam direct-write lithography for integrated circuit manufacturing at the 22 nm node and beyond. This effort will cover a range of topics, including tool assessment, patterning and process integration, as well as data handling and cost of ownership studies.

Brion wins multiyear contract

Brion Technologies, a division of ASML, has reached a multiyear agreement to supply Chartered Semiconductor with a suite of computational lithography products. Chartered will use Brion's Tachyon range of products — in particular the Tachyon OPC+ (optical proximity correction), the Tachyon LMC (lithography manufacturability check), and Tachyon resolution enhancement products — to design and manufacture devices at the 45 nm node and below.

Chartered expects to achieve higher yields by improving the linewidth control using Brion computational technology. Meeting the imaging requirements of advanced technology nodes will require the effective use of increasingly complex resolution enhancement techniques. Chartered will have access to Brion's double-patterning solutions, resolution enhancement techniques and computational lithography solutions. Brion says that the flexibility of its double-patterning schemes allows Chartered to select the optimum combination of techniques for every layer within each design, thus helping to minimize lithography costs.

Collaboration tackles 3D integration

German company SUSS MicroTec and the Taiwanese Industrial Technology Research Institute (ITRI) are to collaborate on the development of 3D integration technologies for semiconductor circuitry. The Advanced Stacked-System Technology and Application Consortium (Ad-STAC), a multinational research association led by ITRI, will implement a variety of SUSS's equipment for processing 300-mm-diameter wafers in a demo production line at ITRI in Hsin-Chu, Taiwan. The equipment includes SUSS's 300 mm lithography cluster LithoPack300 and its 300 mm bond cluster CBC300.

The Ad-STAC consortium is comprised of 12 multinational companies involved in 3D research and development. The LithoPack300 integrates two latest-generation 300 mm photolithography modules — the ACS300 Gen3 spray coater and the MA300 Gen2 mask aligner — in one system. The CBC300 is a modular wafer bonding platform configured to use the latest fusion bonding techniques such as plasma activation and thermo-compression for 3D integration. It offers temporary bonding capability using latest-generation adhesives specifically designed for 3D applications.

"We are proud to have become part of this important alliance in ITRI's Ad-STAC program," stated Frank Averdung, CEO and president of SUSS MicroTec. "We will be working with worldwide leading research and industry partners on viable production platforms to enable cost-efficient and high-yield manufacturing processes."

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